Product Specification

Customer:
Approved by

1. Basic Specifications

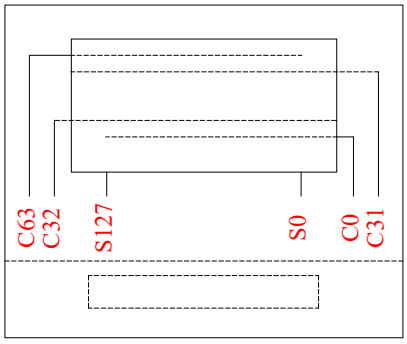
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Blue)
3) Drive Duty: 1/64 Duty

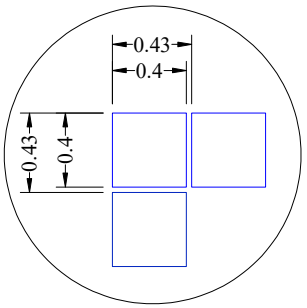
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 128 × 64
3) Panel Size: 60.5 × 37 × 1.8 (mm)
4) Active Area: 55.01 × 27.49 (mm)
5) Pixel Pitch: 0.43× 0.43 (mm)
6) Pixel Size: 0.4 × 0.4 (mm)
7) Weight: TBD

1.3 Active Area / Memory Mapping & Pixel Construction

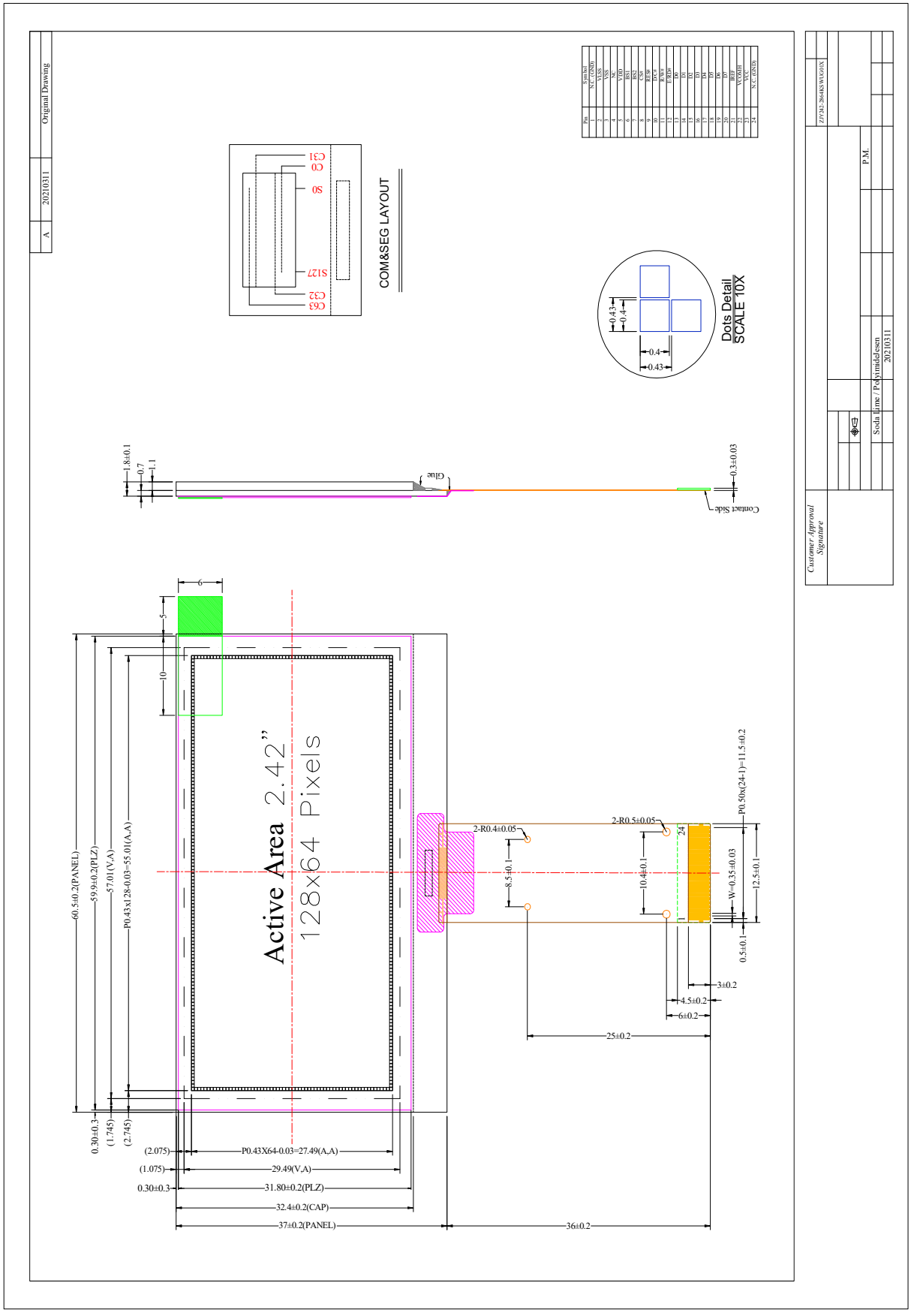


COM&SEG LAYOUT



Dots Detail
SCALE 10X

1.4 Mechanical Drawing



1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>5</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>23</td><td>VCC</td><td>P</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.</td></tr>
<tr><td>2</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to V_{SS} externally.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>9</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>6
7</td><td>BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS1</th><th>BS2</th></tr>
<tr><td>I^2C</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>9</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>8</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>10</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>12</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial or I^2C mode is selected, this pin must be connected to V_{SS}.</td></tr>
<tr><td>11</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial or I^2C mode is selected, this pin must be connected to V_{SS}.</td></tr>
<tr><td>13~20</td><td>D0~D7</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I^2C mode is selected, D2 & D1 should be tired together and serve as SDA_{out} & SDA_{in} in application and D0 is the serial clock input SCL.
Unused pins must be connected to V_{SS} except for D2 in serial mode.</td></tr>
</table>

Driver			
21	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.
22	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
Reserve			
1, 4, 24	N.C. (GND)	-	**Reserved Pin (Supporting Pin)** The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	8	17	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (220 cd/m^2)		13,000	-	hour	4(1)
Life Time (200 cd/m^2)		15,000	-	hour	4(2)
Life Time (180 cd/m^2)		16,000	-	hour	4(3)

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: (1) Setting of 220 cd/m2 :
- Contrast setting : 0x44
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 200 cd/m2 :
- Contrast setting : 0x3e
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 180 cd/m2 :
- Contrast setting : 0x37
- Frame rate : 105Hz
- Duty setting : 1/64

3. Optics & Electrical Characteristics

3.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}		12	12.5	13	V
High Level Input	V_{IH}		$0.8\times V_{DD}$	-	-	V
Low Level Input	V_{IL}		-	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.9\times V_{DD}$	-	-	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	-	-	$0.1\times V_{DD}$	V
VDD Supply Current VDD =2.8V, VCC = 12, IREF = 10uA , No Panel attached, Display ON, All ON,	I_{DD}	Contrast = FFh	-	90	110	μA
VCC Supply Current VDD = 2.8V, VCC =12, IREF =10uA, No Panel attached, Display ON, All ON	I_{CC}		-	450	580	μA
Segment Output Current, VDD = 2.8V, VCC =12V, IREF=10uA, Display ON.	I_{SEG}	Contrast=FFh	280	310	340	μA
		Contrast=AFh	-	215	-	
		Contrast=7Fh	-	155	-	
		Contrast=3Fh	-	78	-	
		Contrast=0Fh	20		-	
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$	VDD = 1.65V~3.3V, VCC = 7V~16V Display OFF, No panel attached	-	-	10	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$	VDD = 1.65V~3.3V, VCC = 7V~16V Display OFF, No panel attached	-	-	10	μA

3.2 Electrical Specifications

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Normal mode current consumption		All pixels on	-	43	52	mA
Standby mode current consumption		Standby mode 10% pixels on	-	0.5	1.5	mA
Normal mode power consumption		All pixels on	-			mW
Standby mode power consumption		Standby mode 10% pixels on	-	6.5	19.5	mW
Brightness	L_{br}	-	90	110	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.24 0.28	0.28 0.32	0.32 0.36	
Dark Room Contrast	CR	-	2000:1	-	-	
Viewing Angle		-	160	-	-	degree

*Note:
VDD is 2.8V,set VDD selection (0xad)=(0x40),
VDD is 1.8V,set VDD selection (0xad)=(0x60) contrast setting is shown below.

(1) Normal mode condition :
- Driving Voltage : 12V
- Contrast setting : 0x3e
- Frame rate : 105Hz
- Duty setting : 1/64

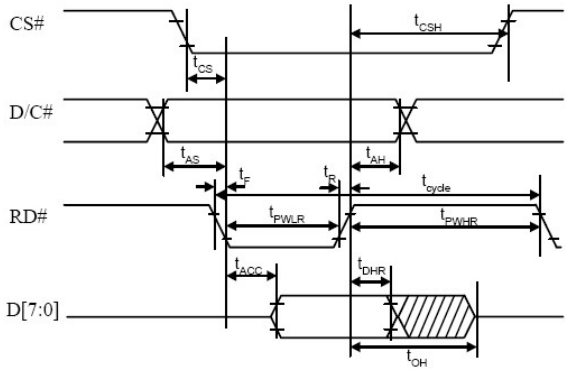
(2) Standby mode condition :
- Driving Voltage : 12V
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/64

3.3 AC Characteristics

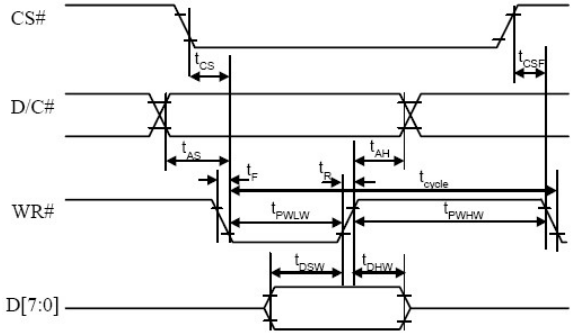
3.3.1.1 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, VDD=VDDIO, T_a = 25°C)



(***Read Timing***)

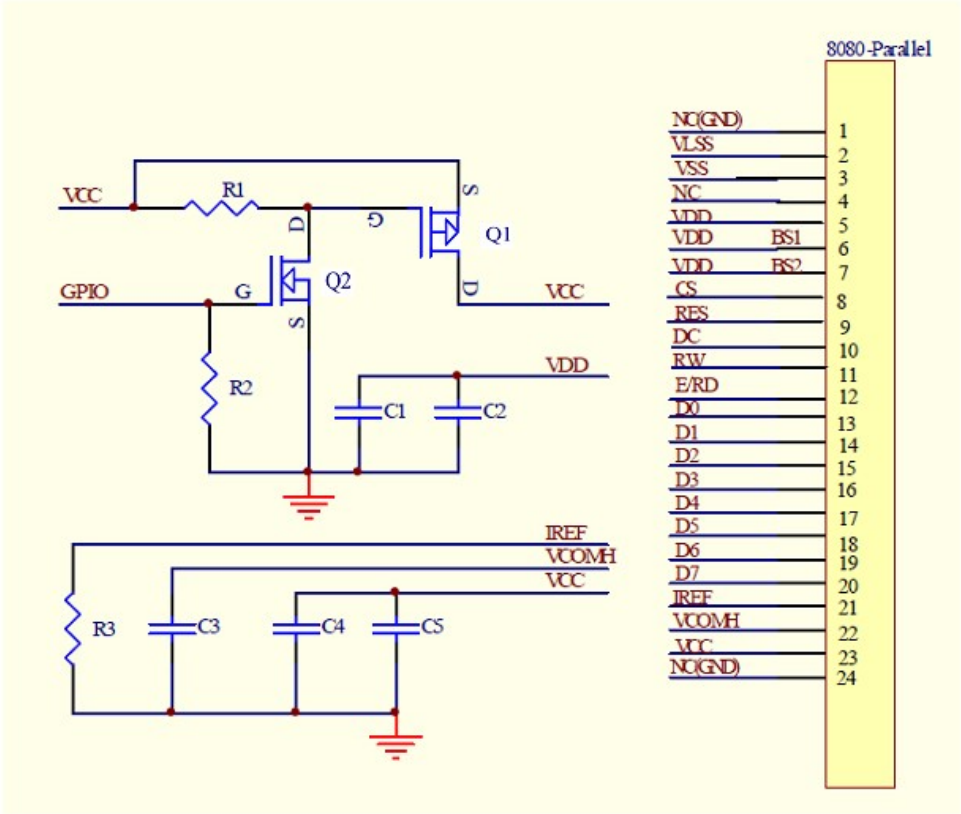


(***Write Timing***)

3.3.1.2 **80XX-Series MPU Parallel Interface**

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2:	1μF / 16V, X5R
C3:	2.2μF /25V
C4:	4.7μF / 25V, X7R
C5:	0.1μF/ 25V, X7R
R1, R2:	47kΩ
R3:	910KΩ, R3 = (Voltage at IREF - VSS) / IREF
Q1:	FDN338P
Q2:	FDN335N

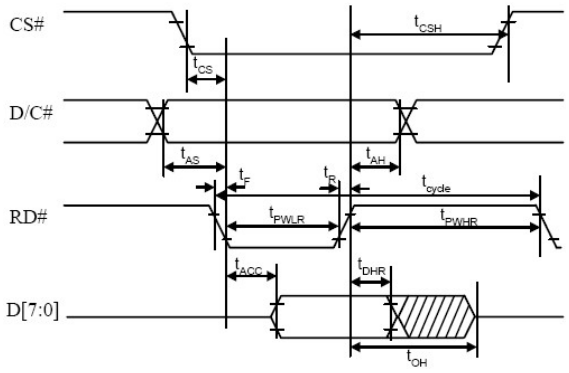
Notes:

VDD:	1.65V~3.3V
VCC_IN:	11.5~12.5V

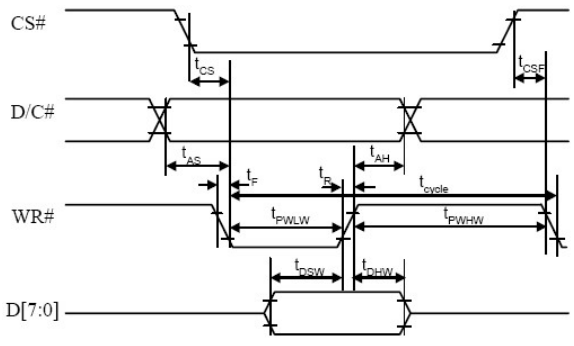
3.3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, VDD=VDDIO, T_a = 25°C)



(***Read Timing***)

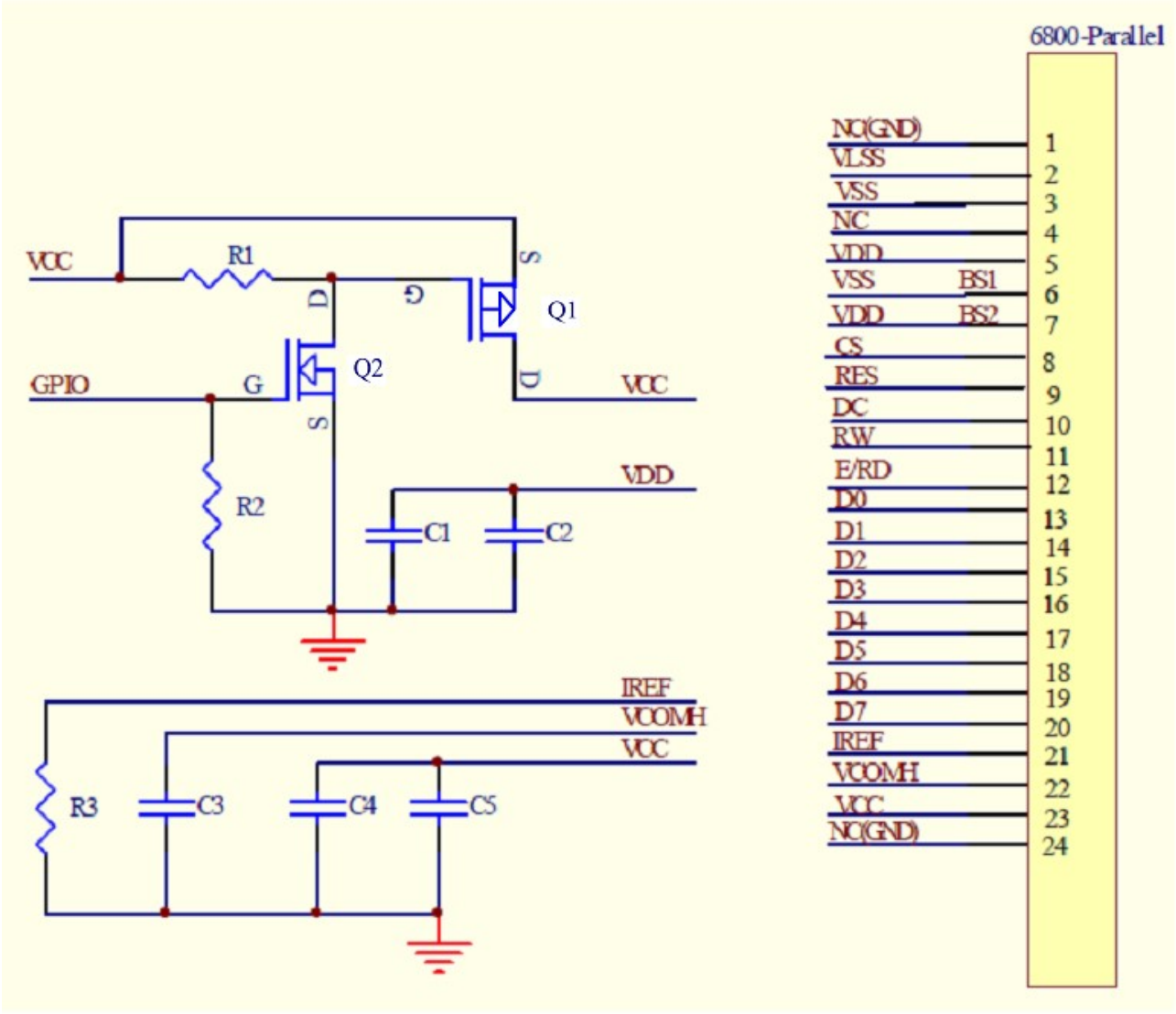


(***Write Timing***)

3.3.2.2 **68XX-Series MPU Parallel Interface**

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2:	1μF / 16V, X5R
C3:	2.2μF /25V
C4:	4.7μF / 25V, X7R
C5:	0.1μF/ 25V, X7R
R1, R2:	47kΩ
R3:	910KΩ, R3 = (Voltage at IREF - VSS) / IREF
Q1:	FDN338P
Q2:	FDN335N

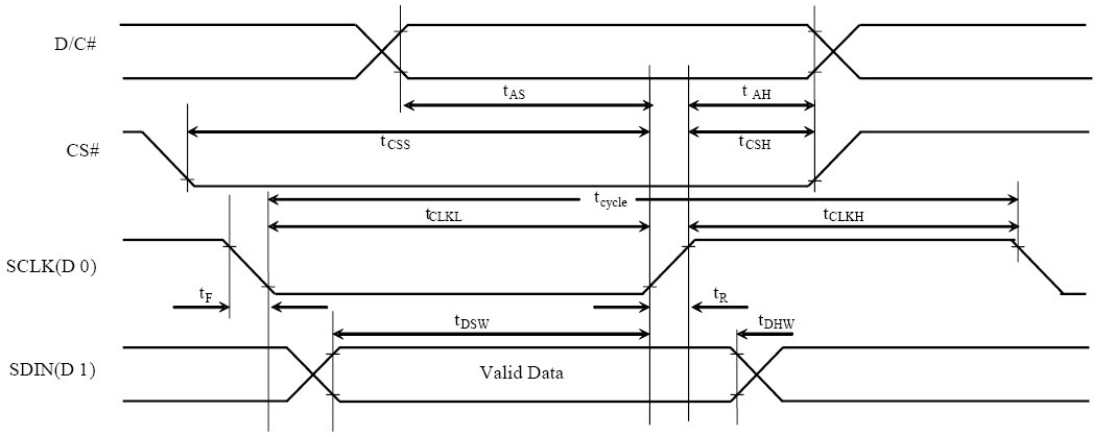
Notes:

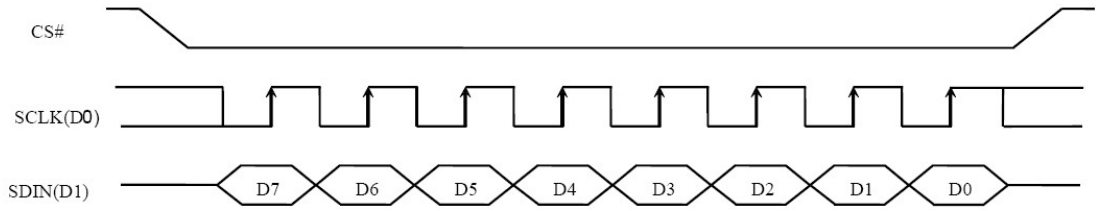
VDD:	1.65V~3.3V
VCC_IN:	11.5~12.5V

3.3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, VDD=VDDIO,T_a = 25°C)

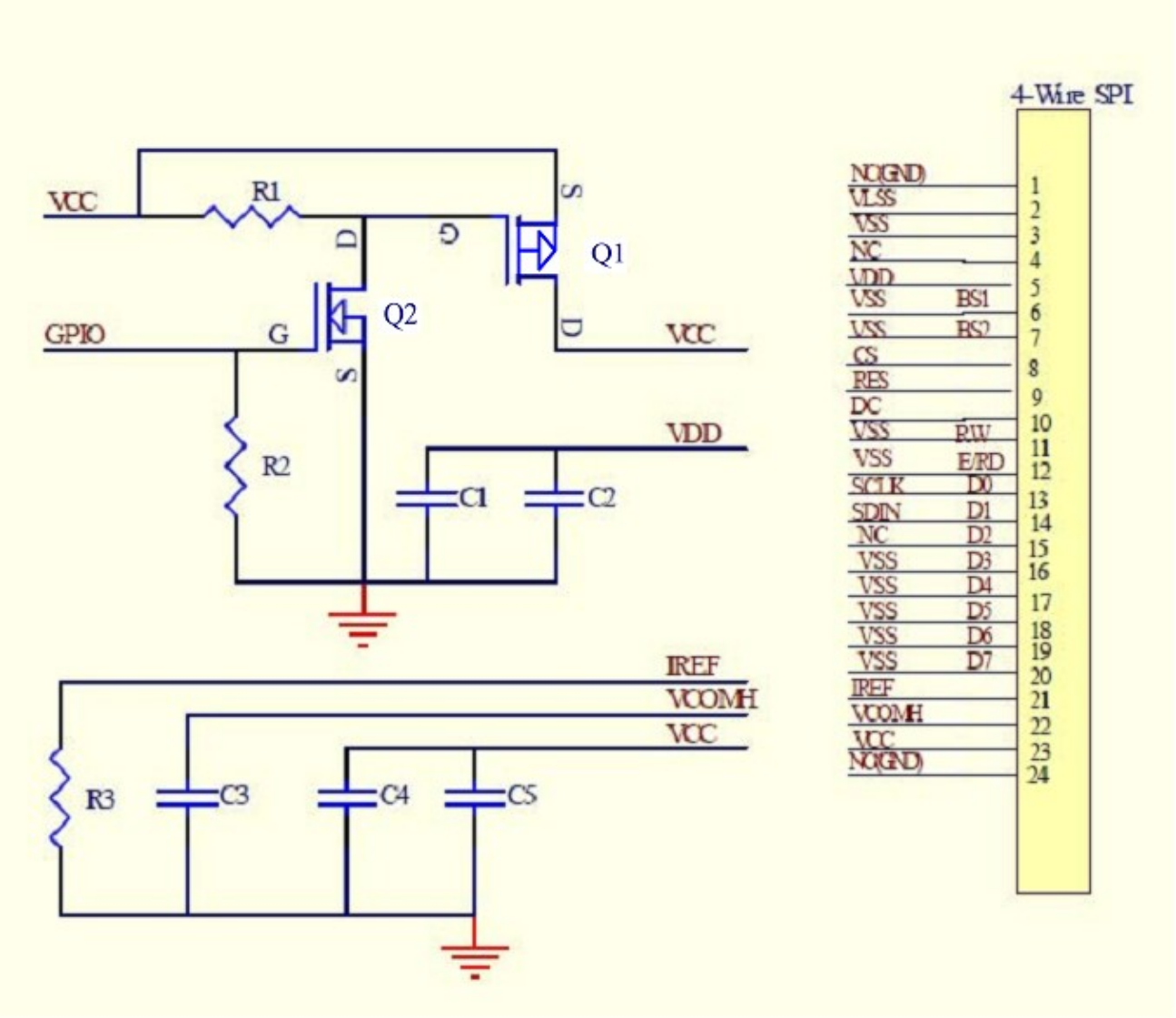




3.3.3.2 **4-wire Serial Interface**

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2: 1μF / 16V, X5R
C3: 2.2μF /25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF/ 25V, X7R
R1, R2: 47kΩ
R3: 910KΩ, R3 = (Voltage at IREF - VSS) / IREF
Q1: FDN338P
Q2: FDN335N

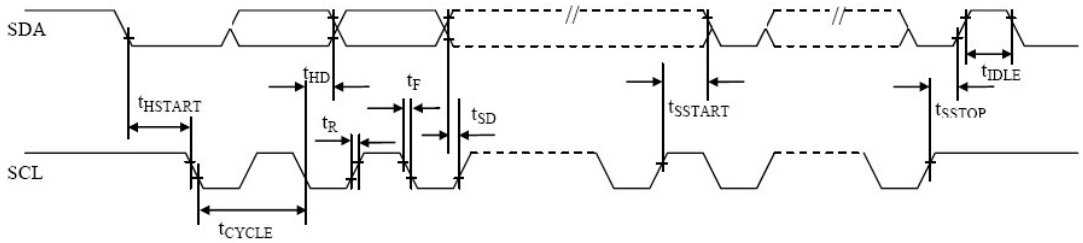
Notes:

VDD: 1.65V~3.3V
VCC_IN: 11.5~12.5V

3.3.4.1 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

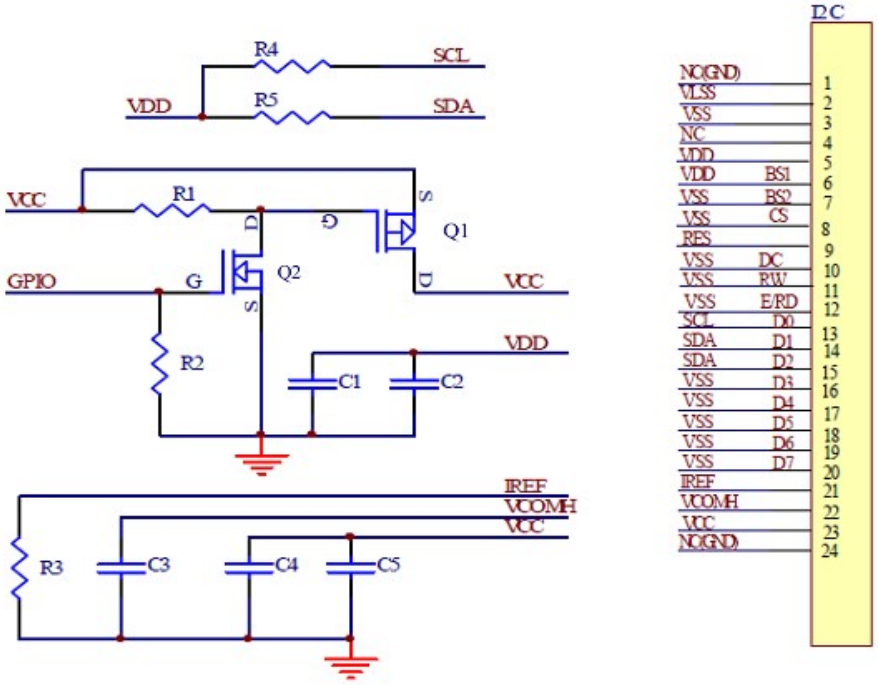
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



3.3.3.2 I²C Interface

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C2: 1μF / 16V, X5R
C3: 2.2μF /25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF/ 25V, X7R
R1, R2: 47kΩ
R3: 910KΩ, R3 = (Voltage at IREF - VSS) / IREF
R4, R5: 4.7kΩ
Q1: FDN338P
Q2: FDN335N

Notes:

VDD: 1.65V~3.3V
VCC_IN: 11.5~12.5V
The I²C slave address is 0111100b'. If the customer ties D/C# to VDD, the I²C slave address will be 0111101b'.

4. Functional Specification

4.1 Commands

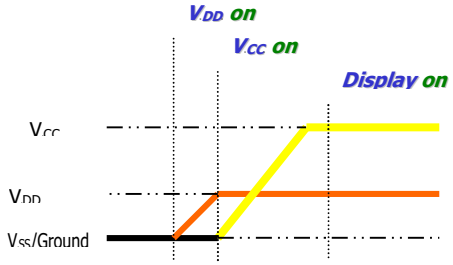
Refer to the Technical Manual for the SSD1309

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

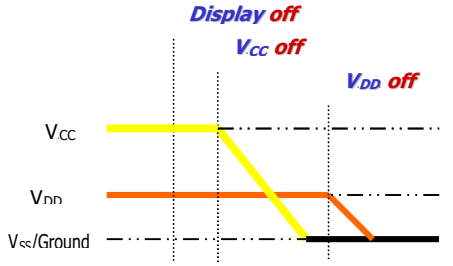
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

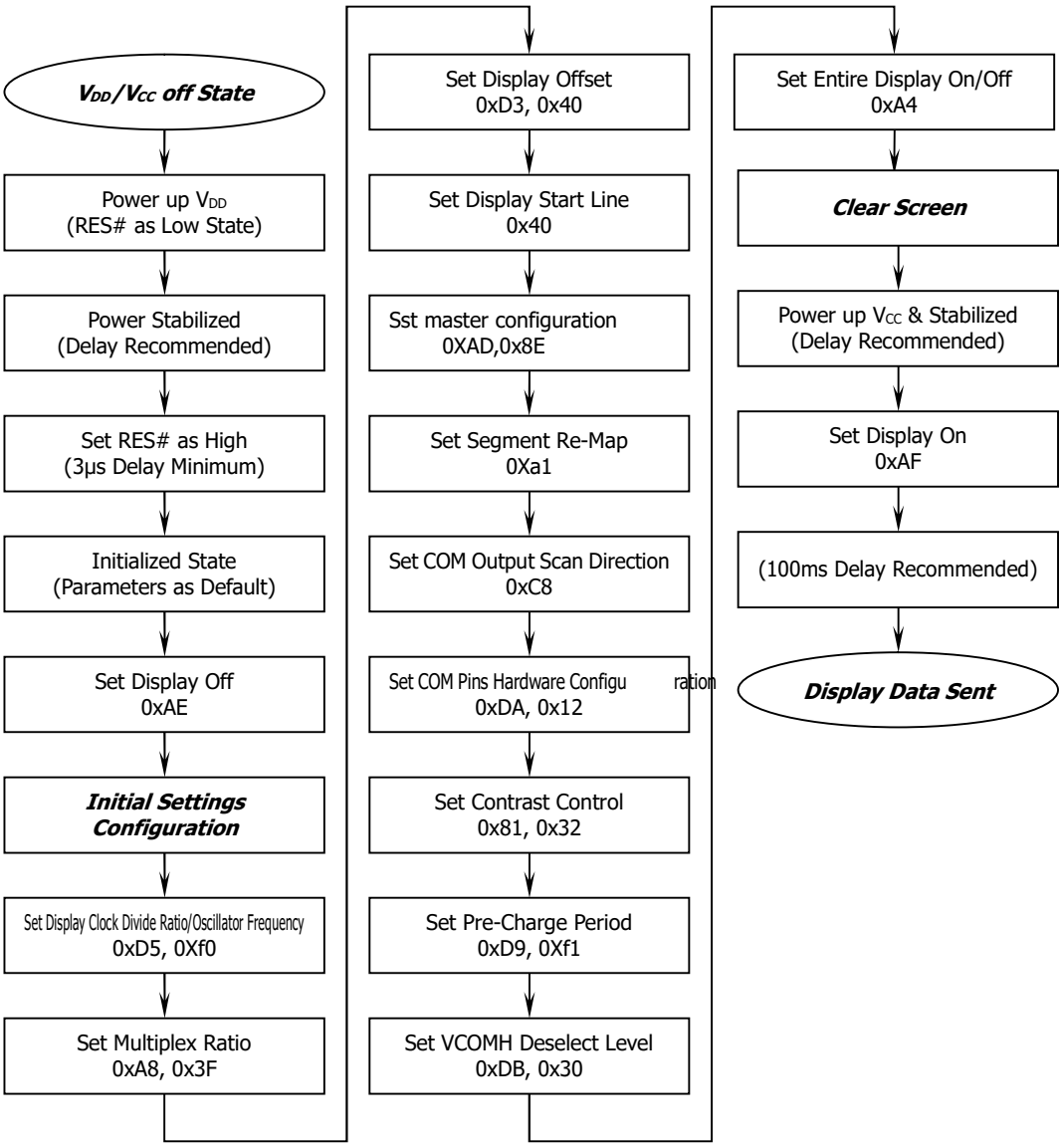
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

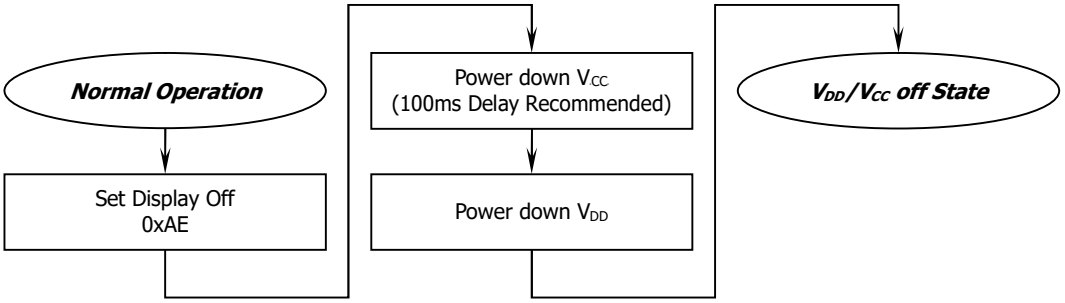
4.4.1 V_{CC} Supplied Externally

<Power up Sequence>

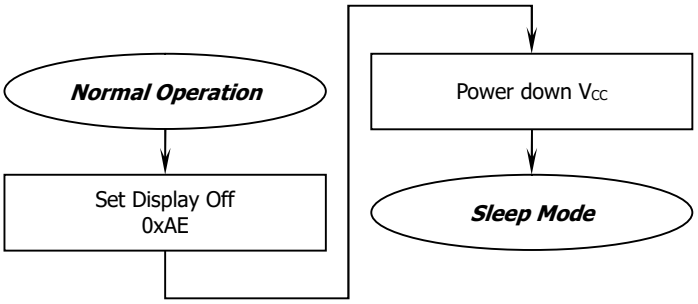


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

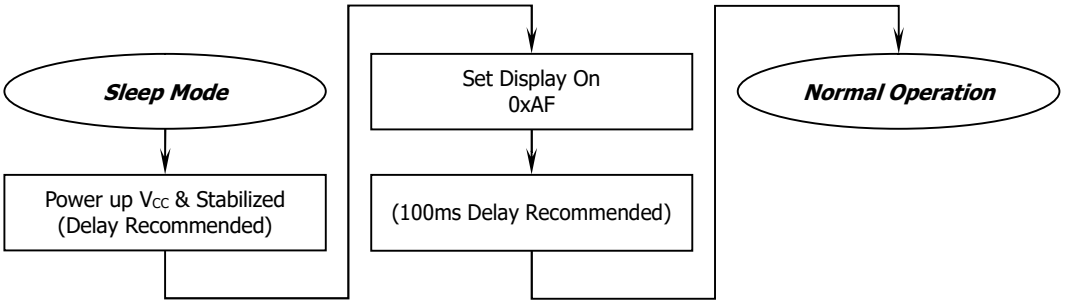
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

```
  void SSD1309 ()
  {
      RES=0;
      delay(1000);
      RES=1;
      delay(1000);

      write_i(0xae); /* set   display off */

      write_i(0x00); /* set   lower column start address */
      write_i(0x10); /* set   higher column start address */

      write_i(0x40); /* set   display start line */

      write_i(0x81); /* set   contrast control */
      write_i(0x32);
```

```
    write_i(0xa1); /* set    segment remap    */

    write_i(0xa6); /* set    normal display */

    write_i(0xa8); /* set    multiplex ratio */
    write_i(0x3f); /* 1/64 */

    write_i(0xc8); /* set    com scan direction */

    write_i(0xd3); /* set    display offset    */
    write_i(0x00);

    write_i(0xd5); /* set    display clock divide/oscillator frequency */
    write_i(0xa0);

    write_i(0xD9);
    write_i(0xF1);

    write_i(0xda); /* set    com pin configuartion */
    write_i(0x12);

    write_i(0x91);
    write_i(0x3F);
      write_i(0x3F);
         write_i(0x3F);
           write_i(0x3F);

    write_i(0xaf); /* set    display on */
}

void write_i(unsigned char ins)
{
    RS=0;
    CS=0;
    WR=0;
    P1=ins;
    WR=1;
    CS=1;
}

void write_d(unsigned char dat)
{
    RS=1;
    CS=0;
    WR=0;
    P1=dat;
    WR=1;
    CS=1;
}
```

```
void delay(unsigned int i)
{
    while(i>0)
        {
        i--;
        }
}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C,120 hrs	
High Temperature Storage	85°C, 120 hrs	
Low Temperature Storage	-40°C, 120 hrs	
High Temperature/Humidity Operation	65°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit/3min) 1cycle: 66min, 100 cycles	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.