Product Specification

Customer:
Approved by

1. Basic Specifications

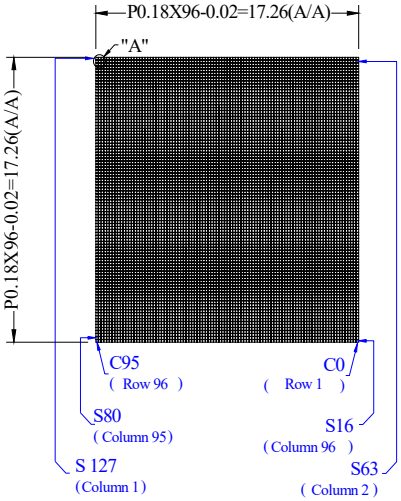
1.1 Display Specifications

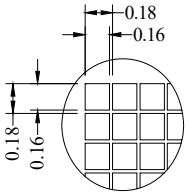
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/96 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 96 × 96
3) Panel Size: 24 × 25.7 × 1.2 (mm)
4) Active Area: 17.26 × 17.26 (mm)
5) Pixel Pitch: 0.18 × 0.18 (mm)
6) Pixel Size: 0.16 × 0.16 (mm)
7) Weight: TBD

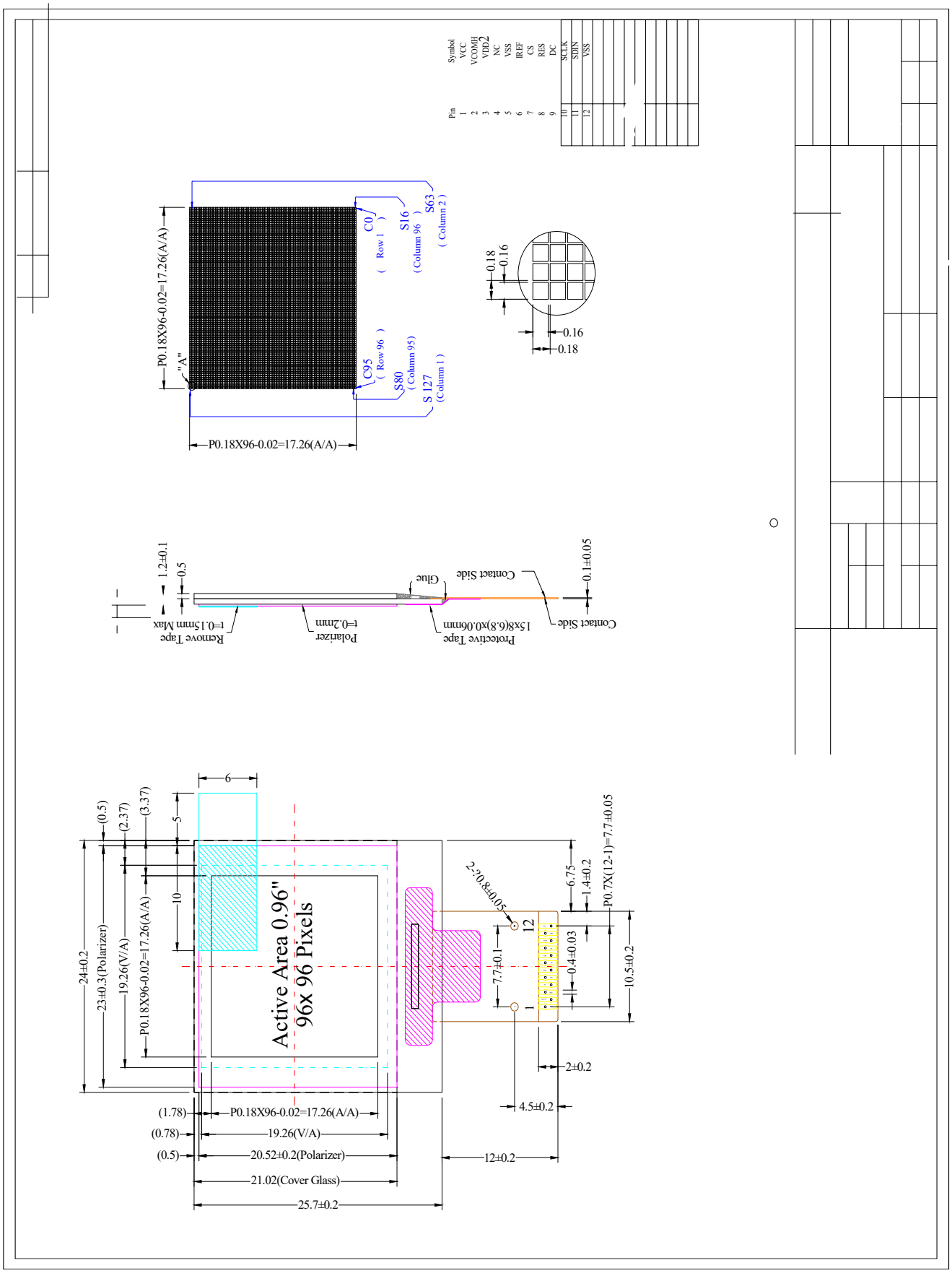
1.3 Active Area / Memory Mapping & Pixel Construction





Detail "A"
Scale (10:1)

1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
3	VDD	P	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
5，12	VSS	P	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
1	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.
7	N.C.	-	**Reserved Pin** The N.C. pin between function pins are reserved for compatible and flexible design.
Driver			
6	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.
2	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
Interface			
8	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
10	SCLK	I	**Serial Clock Input Singal** The transmission if information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
11	SDIN	I/O	**Serial Data Input Signal** This pins acts as a communication channel. The input data through SDIN are latch at the rising edge of SCLK in fhe sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock. SDIN is identified to display data or command by D/C bit data at the rising of first SCLK.
7	CS	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
9	D/C	I	**Data/Command Control** When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register.

Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	8	19	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (100 cd/m^2)		10,000	-	hour	4
Life Time (90 cd/m^2)		11,000	-	hour	4
Life Time (80 cd/m^2)		12,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 8.0V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC} Supplied Externally)	L_{br}	Note 5	250	300	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.37	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	11.5	12	12.5	V
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	$0.8\times V_{DD}$	-	-	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	-	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.9\times V_{DD}$	-	-	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	-	-	$0.1\times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	220	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	-	34	36	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	-	10	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	-	10	μA

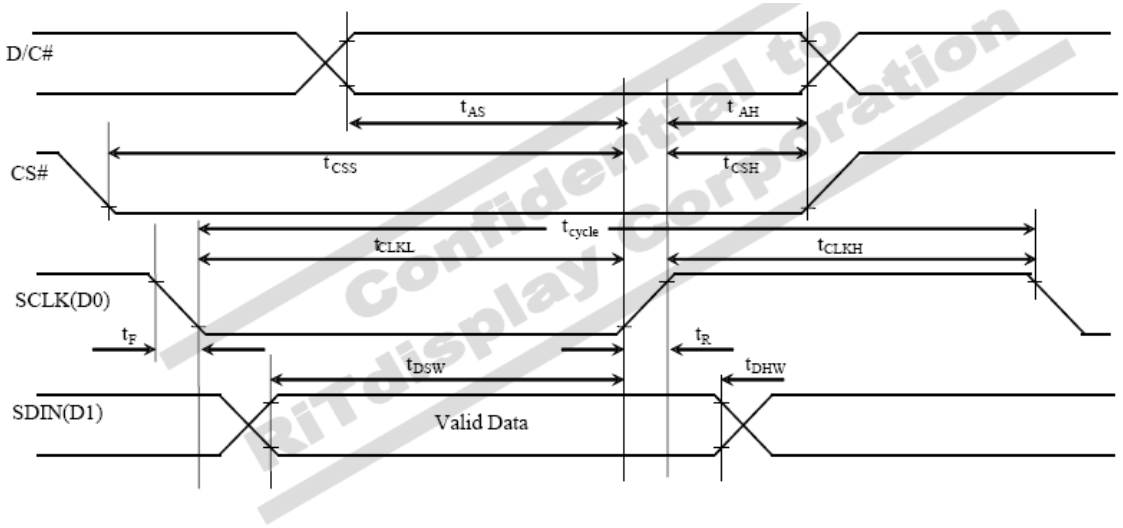
Note 5 & *6*: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 7: V_{DD} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.
*Software configuration follows Section 4.4 Initialization.

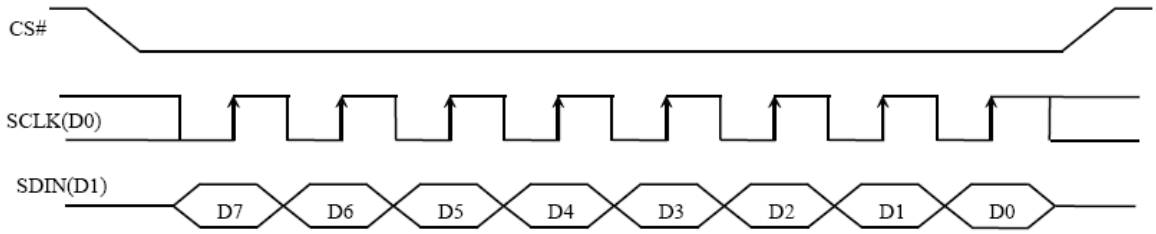
3.3 AC Characteristics

3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
t_{DSW}	Write Data Setup Time	20	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	50	-	ns
t_{CLKH}	Clock High Time	50	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

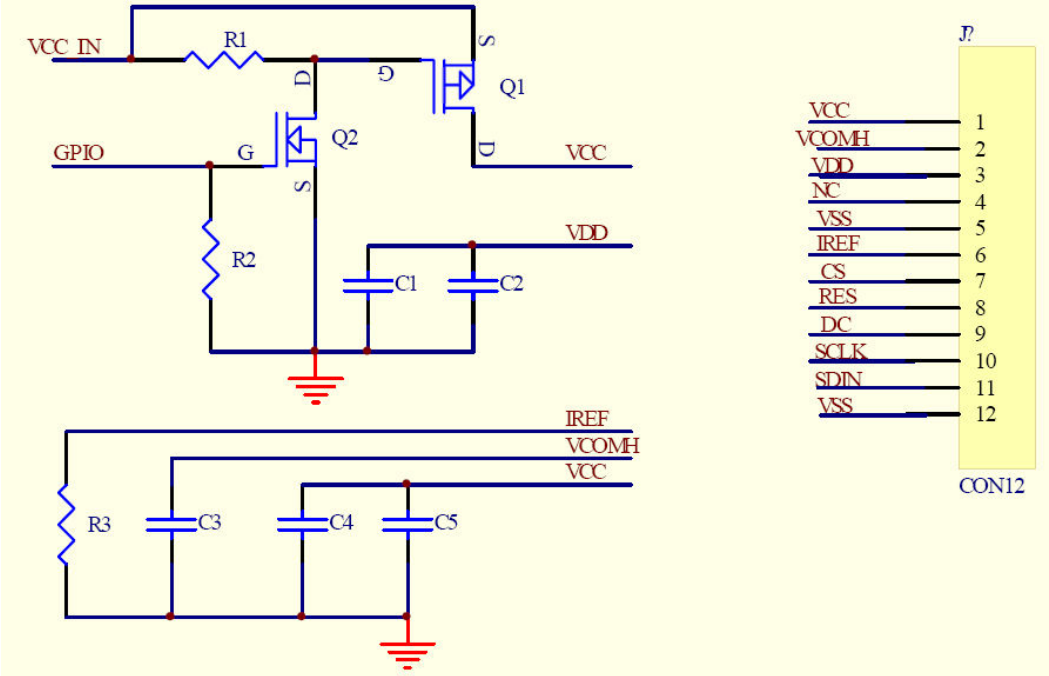




3.3.2 4 wire SPI Interface with External VCC

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	4.7μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.5V, it should be equal to MPU I/O voltage.
VCC_in:	12V

4. Functional Specification

4.1 Commands

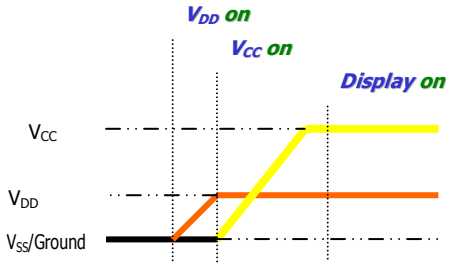
Refer to the Technical Manual for the SSD1317

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

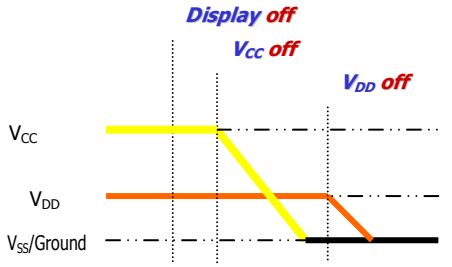
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

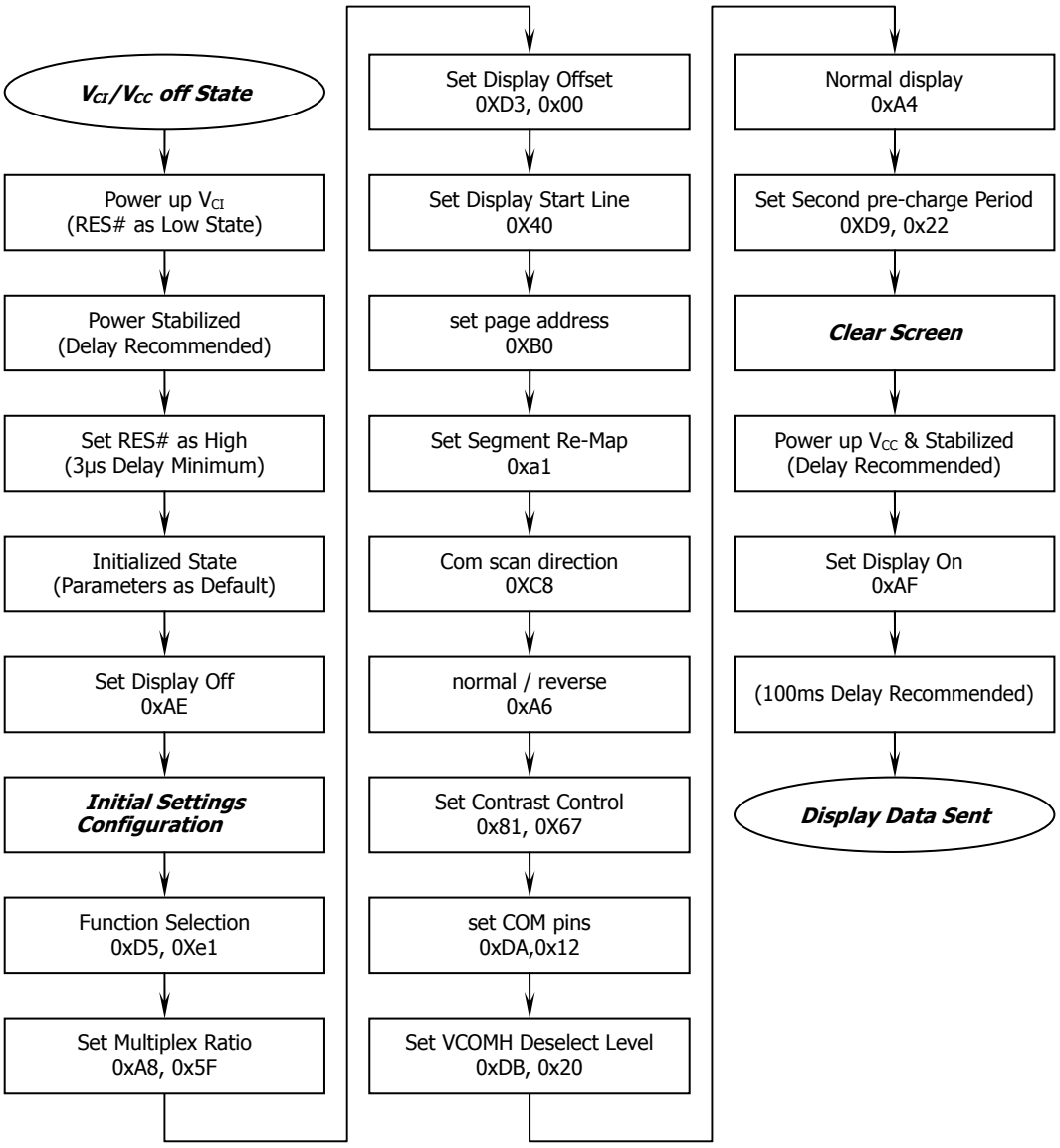
1. Display is OFF
2. 96×96 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 49h
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

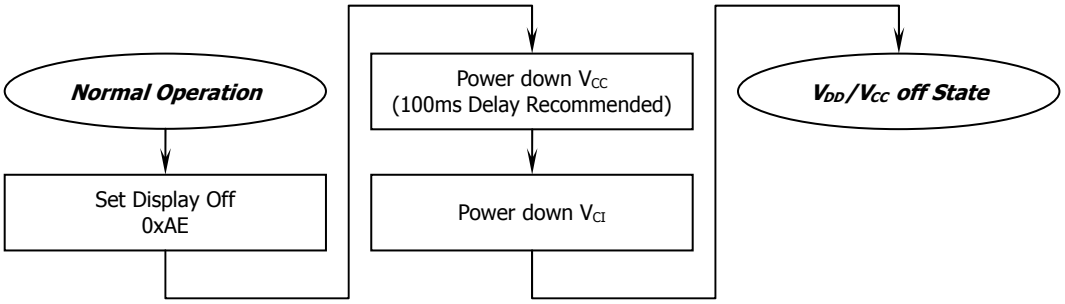
4.4.1 V_{CC} Supplied Externally

<Power up Sequence>

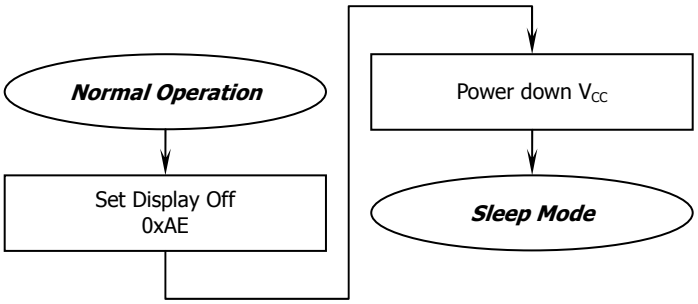


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

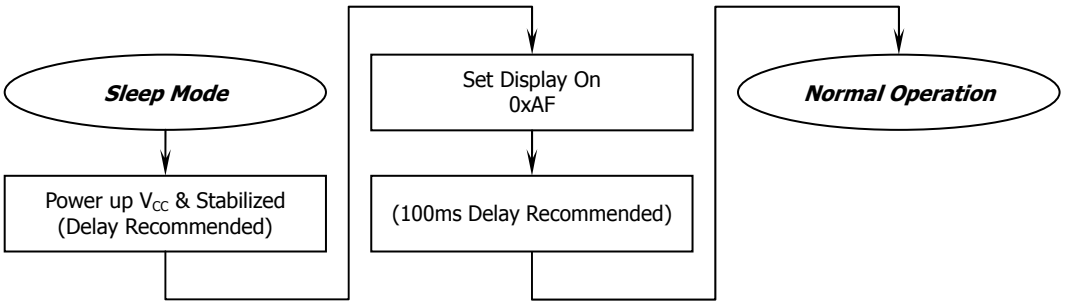
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

```
void   ssd1317()
{
        write_i(0xAE);      /*display off*/

        write_i(0xD5);      /*set osc division*/
        write_i(0xe1);

        write_i(0xA8);      /*multiplex ratio*/
        write_i(0x5F);      /*duty = 1/64*/

        write_i(0xD3);      /*set display offset*/
        write_i(0x00);

        write_i(0x40);      /*set display start line*/

        write_i(0xA1);      /*set segment remap*/
```

```
        write_i(0xC8);      /*Com scan direction*/

        write_i(0xDA);      /*set COM pins*/
        write_i(0x12);

        write_i(0x81);      /*contract control*/
        write_i(0x67);      /*128*/


        write_i(0xD9);      /*set pre-charge period*/
        write_i(0x22);

         write_i(0xdb);      /*set vcomh*/
        write_i(0x20);

        write_i(0xA4);

        write_i(0xA6);      /*normal / reverse*/

        write_i(0xB0);      /*set page address*/

        write_i(0xAF);      /*display ON*/

}

void write_i(unsigned char   ins)
{
  unsigned char   m,da;
  unsigned int j;
      DC=0;
      CS=0;
      da=ins;
  for(j=0;j<8;j++)
     {
       m=da;
       SCL=0;
       m=m&0x80;
       if(m==0x80)
         {
            SDA=1;
          }
        else
          {
               SDA=0;
          }

         da=da<<1;
```

```
          SCL=1;
        }
   CS=1;
}

void write_d(unsigned char   dat)
{
   unsigned char   m,da;
   unsigned int j;
       DC=1;
       CS=0;
       da=dat;
   for(j=0;j<8;j++)
      {
        m=da;
        SCL=0;
        m=m&0x80;
        if(m==0x80)
          {
             SDA=1;
           }
         else
           {
                SDA=0;
           }

          da=da<<1;
          SCL=1;
        }
   CS=1;
}

void delay(unsigned int i)
{
     while(i>0)
     {
     i--;
     }
}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.