Product Specification

Customer:

Approved by

1. Basic Specifications

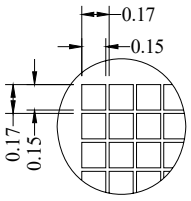
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/80 Duty

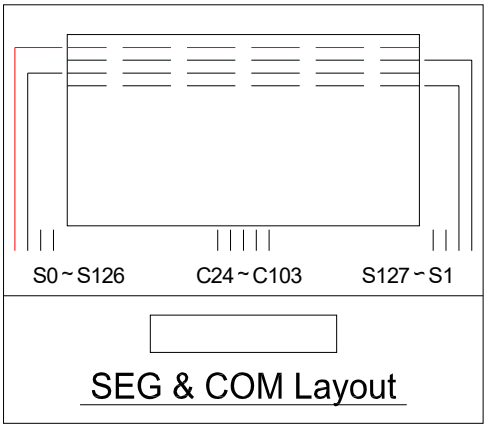
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 128 × 80
3) Panel Size: 12.13 × 23.6 × 1.22 (mm)
4) Active Area: 9.68 × 17.26 (mm)
5) Pixel Pitch: 0.17 × 0.17 (mm)
6) Pixel Size: 0.15 × 0.15 (mm)
7) Weight: TBD

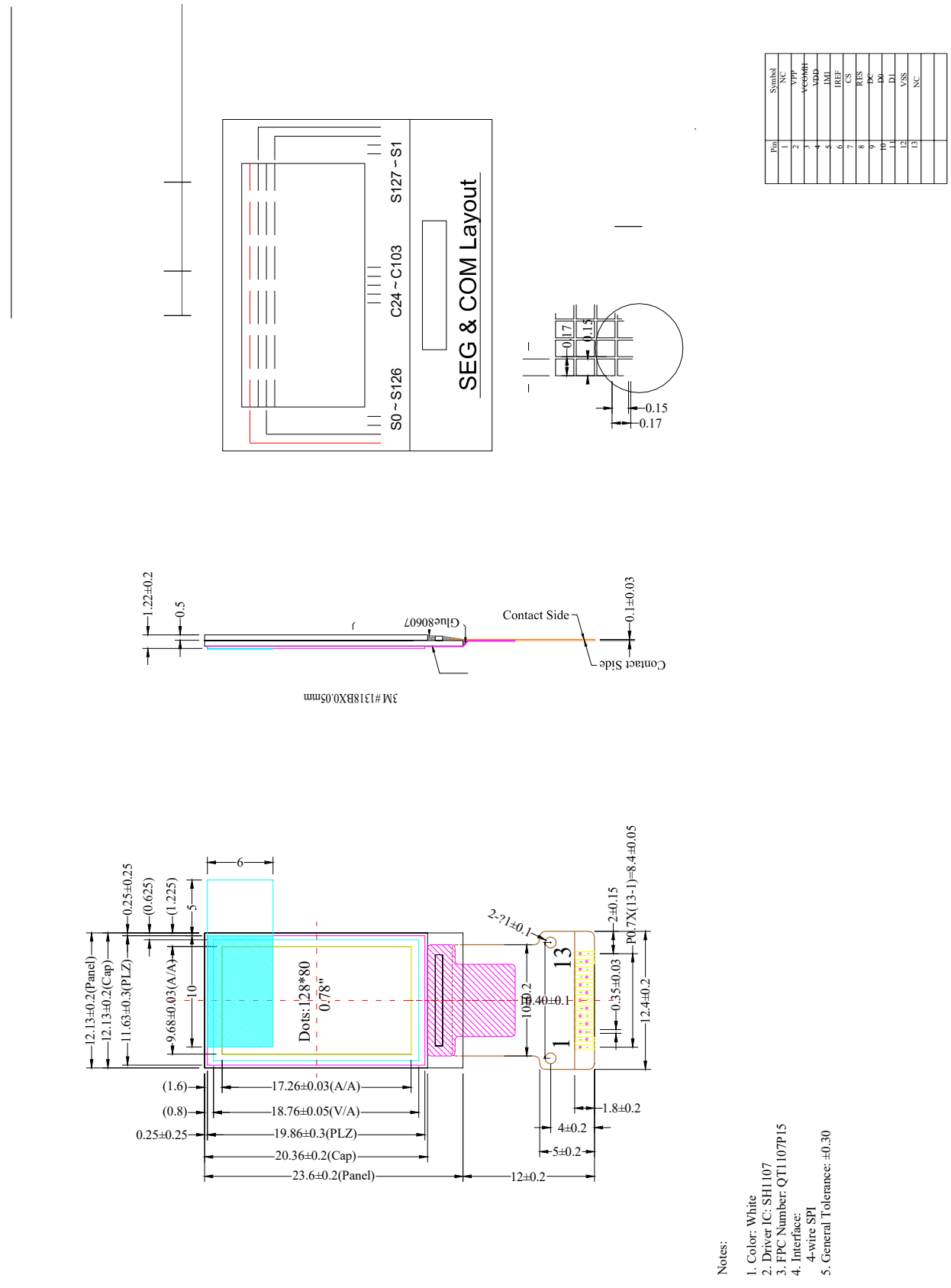
1.3 Active Area / Memory Mapping & Pixel Construction



Detail "A"
Scale (10:1)



1.4 Mechanical Drawing



Notes:

1. Color: White
2. Driver IC: SH1107
3. FPC Number: QT1107P15
4. Interface:
   4-wire SPI
5. General Tolerance: ±0.30

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>2</td><td>VPP</td><td>P</td><td>Power Supply for OEL Panell
This is the most positive voltage supply pin of the chip. It must be supplied externally.</td></tr>
<tr><td>4</td><td>VDD</td><td>P</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>12</td><td>VSS</td><td>P</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>6</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>5</td><td>IM1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>IM1</td></tr>
<tr><td>4-wire SPI</td><td>0</td></tr>
<tr><td>I2C</td><td>1</td></tr>
</table></td></tr>
<tr><td>8</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>7</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>9</td><td>A0</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.
When the pin is pulled high and serial interface mode is selected, the data at SI will be interpreted as data. When it is pulled low, the data at SI will be
transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>10,11</td><td>D0,D1</td><td>I/O</td><td>Serial Data Input/Output and clock
When serial mode is selected, D1 will be the serial data input SI and D0 will be the serial clock input SCL.
When I2C mode is selected, D1 be the serial data input SDA and D0 is the serial clock input, SCL.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1,13</td><td>NC</td><td>-</td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
</table>

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V_{PP}	7	16.5	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (150 cd/m^2)		10,000	-	hour	4

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{PP} Supplied Externally)	L_{br}	Note 4	170	220	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{PP} = 9V.
Software configuration follows Section 4.5 Initialization.

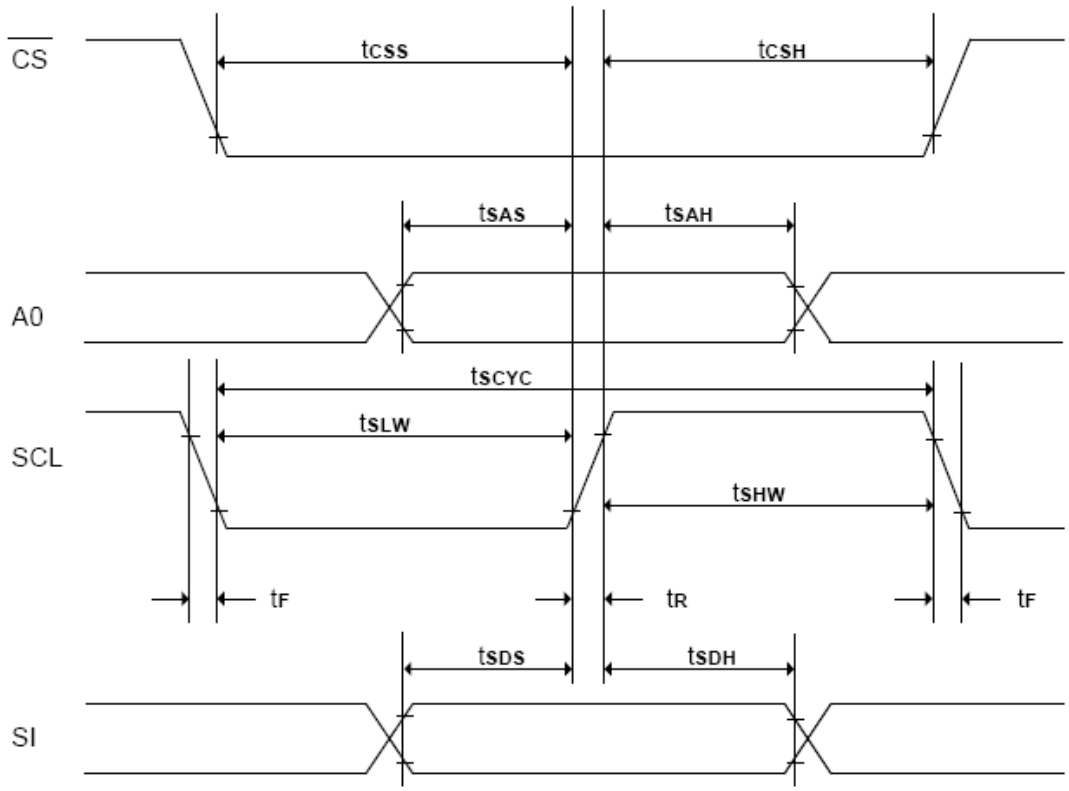
3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.5	V
Supply Voltage for Display	V_{PP}	Note 5	8.5	9.0	9.5	V
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.2\times V_{DD}$	V
Operating Current for V_{CI}	I_{DD}		-	55	100	μA
Operating Current for V_{PP}	I_{PP}	Note 6	-	13	18	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	0.1	5	μA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	0.5	5	μA

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Data Setup Time	200	-	ns
t_{SDH}	Data Hold Time	200	-	ns
t_{CSS}	Chip Select Setup Time	240	-	ns
t_{CSH}	Chip Select Hold Time	120	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

(V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)

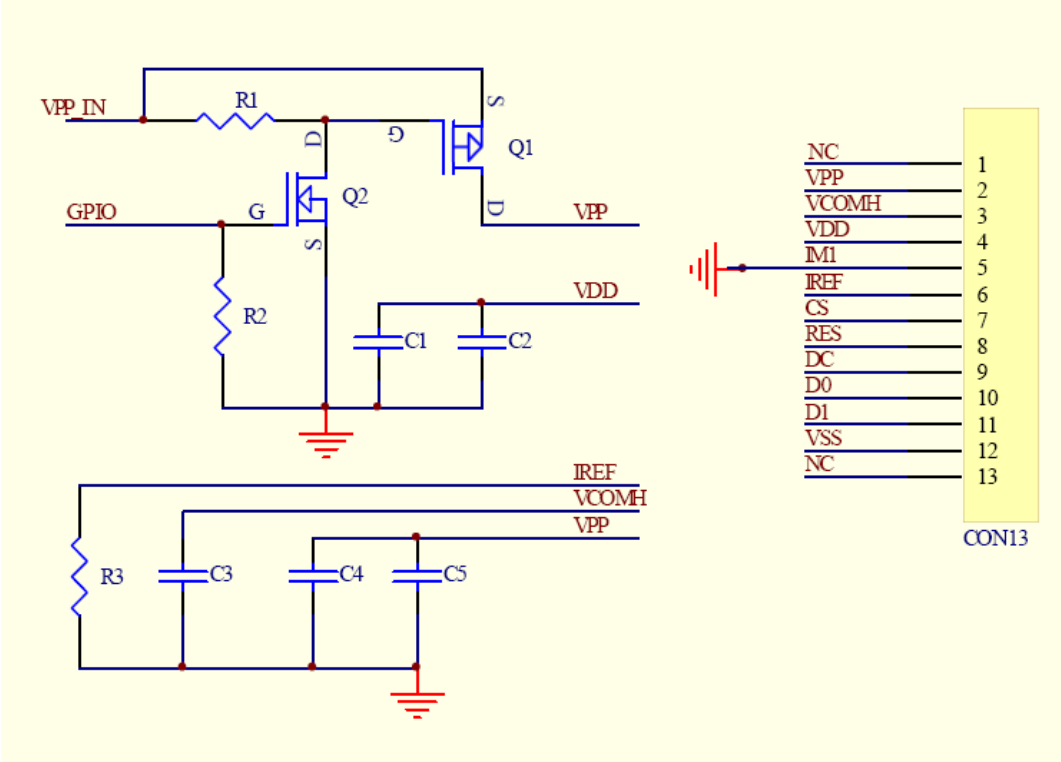
Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Data Setup Time	100	-	ns
t_{SDH}	Data Hold Time	100	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns


CS
tCSS
tCSH
A0
tSAS
tSAH
SCL
tSCYC
tSLW
tSHW
tF
tR
tF
SI
tSDS
tSDH

3.3.3.2 **4-wire Serial Interface**

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
Q1:	FDN338P
Q2:	FDN335N

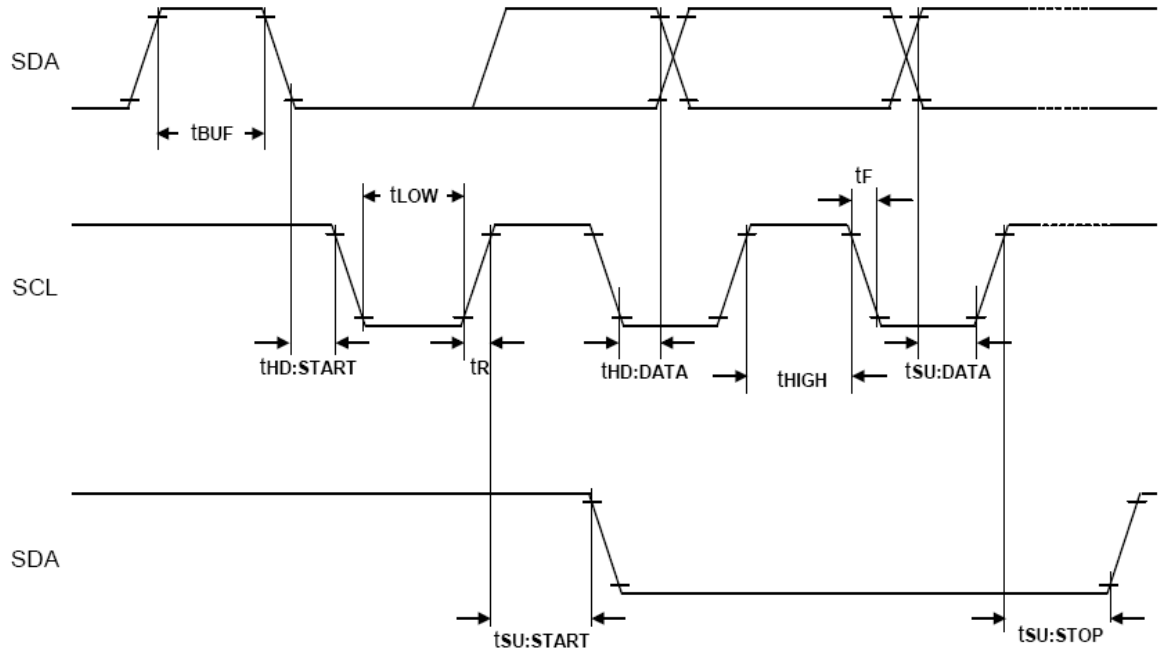
Notes:

VDD:	1.65~3.5V, it should be equal to MPU I/O voltage.
Vpp_in:	8.5~9.5V

3.3.4.1 I2C Interface Timing Characteristics:

(V_{DD} = 1.65 - 3.5V, TA = +25°C)

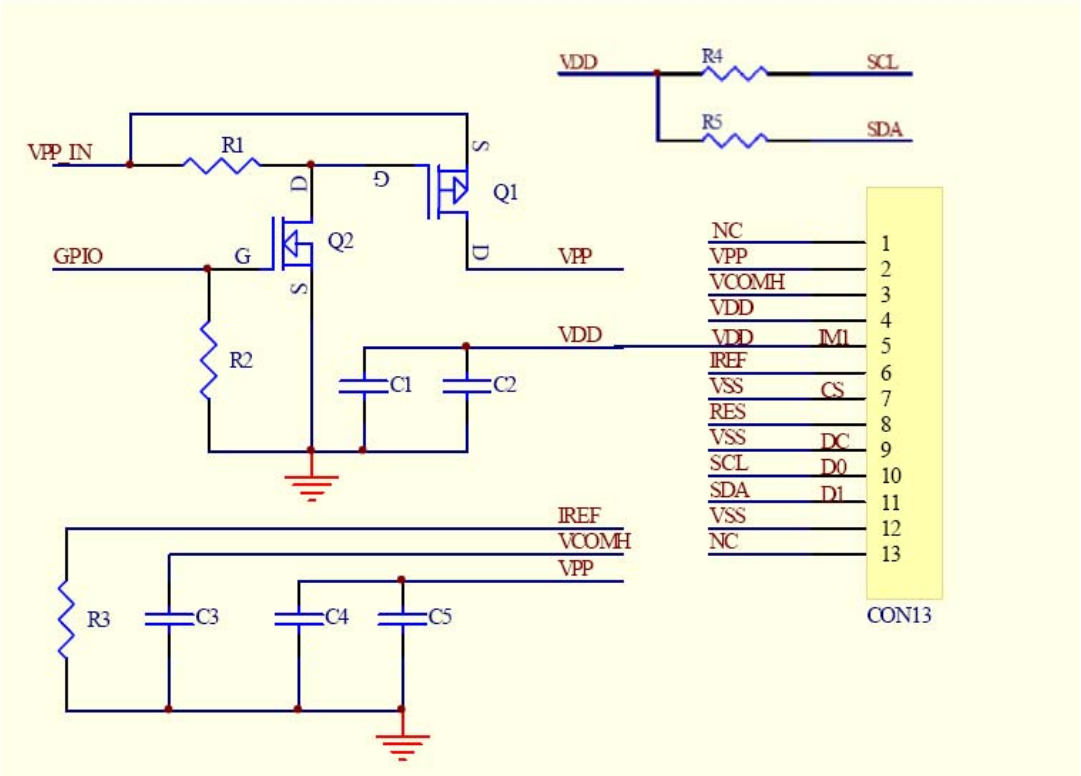
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	kHz	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	μs	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	μs	
$T_{SU:DATA}$	data setup time	100	-	-	ns	
$T_{HD:DATA}$	data hold time	0	-	0.9	μs	
T_R	SCL、SDA rise time	20+0.1Cb	-	300	ns	
T_F	SCL、SDA fall time	20+0.1Cb	-	300	ns	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	μs	
$T_{HD:START}$	START Hold time	0.6	-	-	μs	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	μs	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	μs	



3.3.4.2 I^2C Interface Characteristics

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	4.7μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5 :	4.7 kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.5V, it should be equal to MPU I/O voltage.
Vpp_in:	8.5~9.5V

4. Functional Specification

4.1 Commands

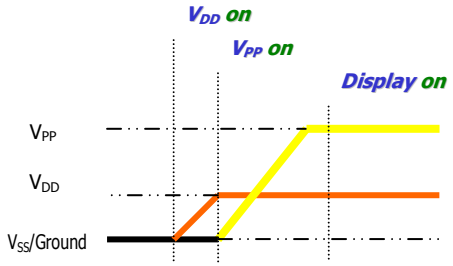
Refer to the Technical Manual for the SH1107

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

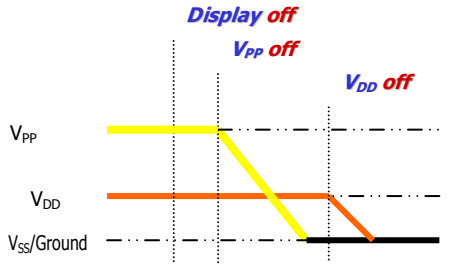
4.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VPP
6. Delay 100ms
(When VPP is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VPP
3. Delay 100ms
(When VPP is reach 0 and panel is completely discharges)
4. Power down VDD



Note 9:

1) Since an ESD protection circuit is connected between VDD and VBPPB inside the driver IC, VPP becomes lower than VDD whenever VBDDB is ON and VPP is OFF.
2) VPPB should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VPP) can never be pulled to ground under any circumstance.
4) VBDDB should not be power down before VPP power down.

4.3 Reset Circuit

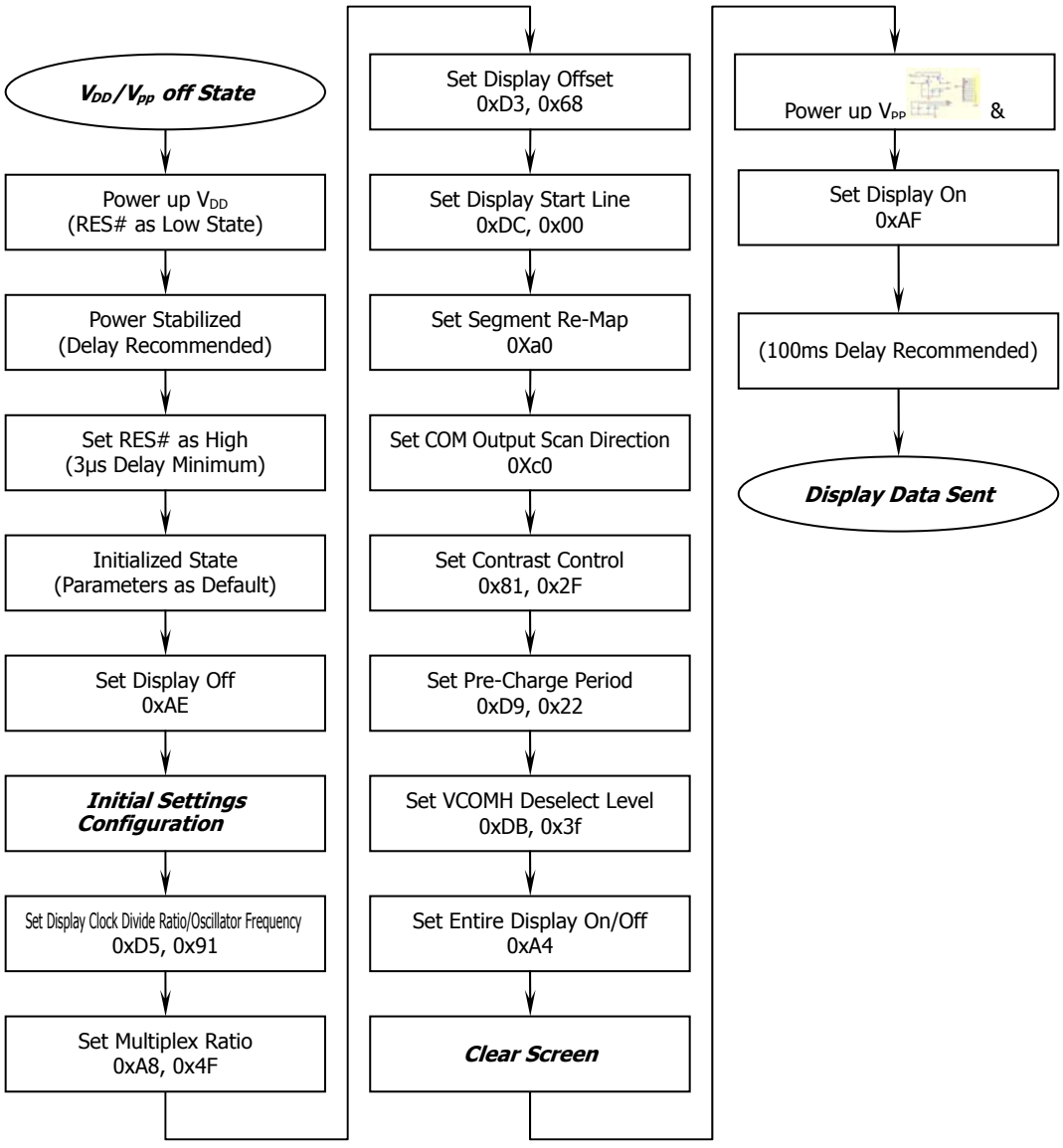
When RESB input is low, the chip is initialized with the following status:

1. Display is OFF. Common and Segment are in high impedance state.
2. 128´128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line
of the display).
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

4.4 Actual Application Example

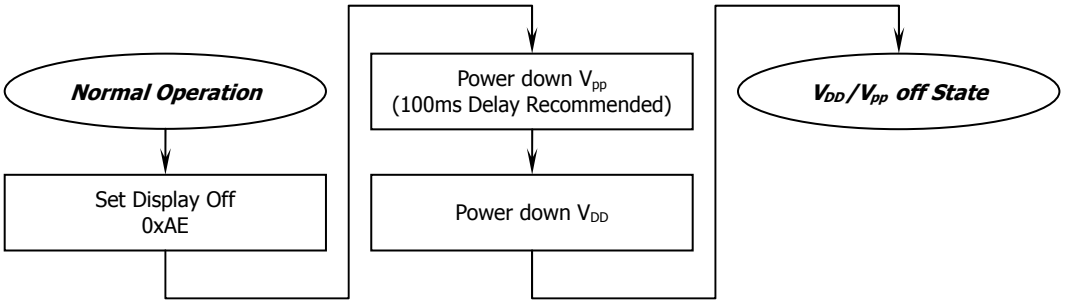
Command usage and explanation of an actual example

4.4.1 V_{pp} Supplied Externally

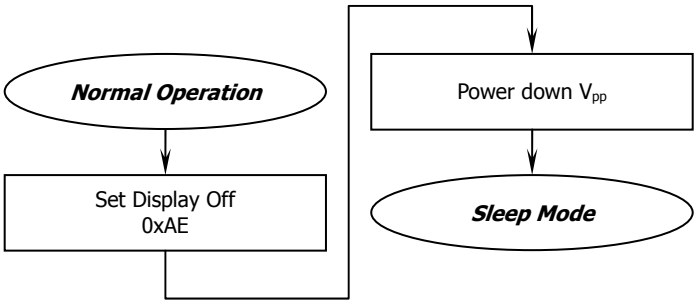


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

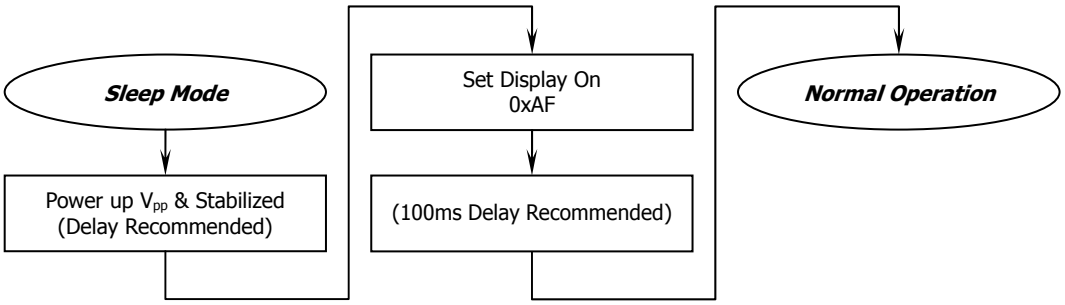
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting
void sh1107()

```
{
        write_i(0xAE);      /*display off*/

        write_i(0x00);      /*set lower column address*/
        write_i(0x10);      /*set higher column address*/

        write_i(0x20);      /* Set Memory addressing mode (0x20/0x21) */

        write_i(0x81);      /*contract control*/
        write_i(0x2f);      /*b0*/

        write_i(0xA0);      /*set segment remap*/

        write_i(0xC0);      /*Com scan direction*/

        write_i(0xA4);      /*Disable Entire Display On (0xA4/0xA5)*/

        write_i(0xA6);      /*normal / reverse*/

        write_i(0xD5);      /*set osc division*/
        write_i(0x91);

        write_i(0xD9);      /*set pre-charge period*/
```

```
        write_i(0x22);

        write_i(0xdb);      /*set vcomh*/
        write_i(0x3f);

        write_i(0xA8);      /*multiplex ratio*/
        write_i(0x4F);      /*duty = 1/80*/

        write_i(0xD3);      /*set display offset*/
        write_i(0x68);      /*18*/

        write_i(0xdc);      /*Set Display Start Line*/
        write_i(0x00);

        write_i(0xad);      /*set charge pump enable*/
        write_i(0x8a);       /*Set DC-DC enable (a=0:disable; a=1:enable) */

        write_i(0xAF);      /*display ON*/

}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.